Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An input/output structure for a die to support an Accelerated Graphic Port (AGP) standard and a Peripheral Component Interconnection Express (PCIE) standard, comprising:
a PCIE input/output pad for supporting PCIE standard;
an AGP input/output pad for supporting AGP standard;
a die pad coupled to an external circuit;
a first conducting distributed wire coupled to said PCIE input/output pad and said die pad; and
a second conducting distributed wire coupled to said AGP input/output pad and said die pad;
wherein only one of said PCIE input/output pad and said AGP input/output pad is enabled at the same time.

[c2] 2. The structure of claim 1, wherein said PCIE input/output pad and said AGP input/output pad are controlled by an enable signal so that when said PCIE input/output pad is enabled, said AGP input/output pad is disabled, when said AGP input/output pad is enabled, said PCIE input/output pad is disabled.

[c3] 3. The structure of claim 1, wherein said die pad is coupled to a bonding pad of a substrate via a conducting

wire.

[c4] 4. The structure of claim 1, wherein said first and second conducting distributed wires are in a re-distributed layer.

[c5] 5. An input/output structure for a die to support a plurality of standards, comprising:
a first input/output pad for supporting a first standard;
a second input/output pad for supporting a second standard;
a die pad coupled to an external circuit;
a first conducting distributed wire coupled to said first input/output pad and said die pad; and
a second conducting distributed wire coupled to said second input/output pad and said die pad;
wherein only one of said first input/output pad and said second input/output pad is enabled at the same time.

[c6] 6.The structure of claim 5, wherein said first input/output pad and said second input/output pad are controlled by an enable signal so that when said first input/output pad is enabled, said second input/output pad is disabled, when said second input/output pad is enabled, said first input/output pad is disabled.

[c7] 7. The structure of claim 5, wherein said die pad is cou-

pled to a bonding pad of a substrate via a conducting wire.

[c8] 8. The structure of claim 5, wherein said first and second conducting distributed wires are in a re-distributed layer.